

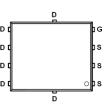
# SSF4006J7

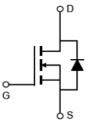
#### Main Product Characteristics:

V <sub>DSS</sub>	40V				
R <sub>DS</sub> (on)	5.3mΩ (typ.)				
I <sub>D</sub>	80A				



PQFN 5x6





Marking and pin Assignment

Schematic diagram

#### **Features and Benefits:**

- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 175°C operating temperature



## **Description:**

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

### **Absolute max Rating:**

Symbol	Parameter	Max.	Units
I <sub>D</sub> @ TC = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V ①	80	Δ
I <sub>DM</sub>	Pulsed Drain Current 2	350	A
P <sub>D</sub> @TC = 25°C	Power Dissipation ③	90	W
V <sub>DS</sub>	Drain-Source Voltage	40	V
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	V
E <sub>AS</sub>	Single Pulse Avalanche Energy @ L=0.5mH	390	mJ
T <sub>J</sub> T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to +175	°C



## **Thermal Resistance**

Symbol	Characterizes	Тур.	Max.	Units
R <sub>θJC</sub>	Junction-to-case ③	_	1.67	°C/W

#### **Electrical Characterizes** $@T_A=25^{\circ}C$ unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source breakdown voltage	40	_	_	V	$V_{GS} = 0V, I_D = 250 \mu A$
R <sub>DS(on)</sub>	Static Drain-to-Source on-resistance	—	5.3	6.5	mΩ	V <sub>GS</sub> =10V,I <sub>D</sub> =20A
V <sub>GS(th)</sub>	Gate threshold voltage	1.2	_	2.5	V	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$
I <sub>DSS</sub>	Drain-to-Source leakage current	_	—	1	μA	$V_{DS} = 40V, V_{GS} = 0V$
		_	_	100	nA	V <sub>GS</sub> =20V
I <sub>GSS</sub>	Gate-to-Source forward leakage		_	-100		V <sub>GS</sub> = -20V
Qg	Total gate charge	_	55	_	nC	I <sub>D</sub> = 20A,
$Q_{gs}$	Gate-to-Source charge	_	18	—		V <sub>DS</sub> =20V,
$Q_{gd}$	Gate-to-Drain("Miller") charge	_	20	_		$V_{GS} = 10V$
t <sub>d(on)</sub>	Turn-on delay time	_	15	_		
t <sub>r</sub>	Rise time	_	12	_	ns	V <sub>GS</sub> =10V, V <sub>DS</sub> =20V,
t <sub>d(off)</sub>	Turn-Off delay time		40	_		$R_{GEN}=3\Omega$
t <sub>f</sub>	Fall time		15	_		$R_L=1\Omega$
C <sub>iss</sub>	Input capacitance	_	3800	_	pF	$V_{GS} = 0V$
C <sub>oss</sub>	Output capacitance	_	700	_		$V_{DS} = 20V$
C <sub>rss</sub>	Reverse transfer capacitance	_	350	_		f = 1MHz

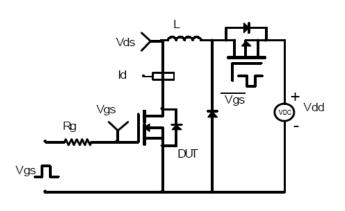
## **Source-Drain Ratings and Characteristics**

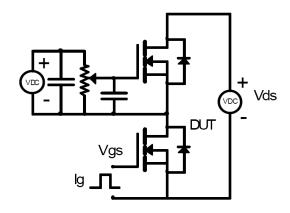
Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions	
I <sub>S</sub>	Continuous Source Current (Body Diode)	_	_	80	A	MOSFET symbol showing the integral reverse p-n junction diode.	
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.2	V	I <sub>S</sub> =10A, V <sub>GS</sub> =0V	
trr	Reverse Recovery Time	—	35	—	ns	I <sub>S</sub> =20A,di/dt=100A/us	
Qrr	Reverse Recovery Charge	—	37	—	nC		



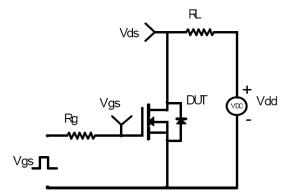
## **Test circuits and Waveforms**

#### EAS Test Circuit:



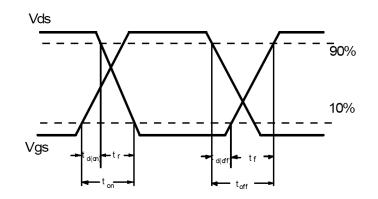


Switching Time Test Circuit:



Switching Waveforms:

Gate charge test circuit:

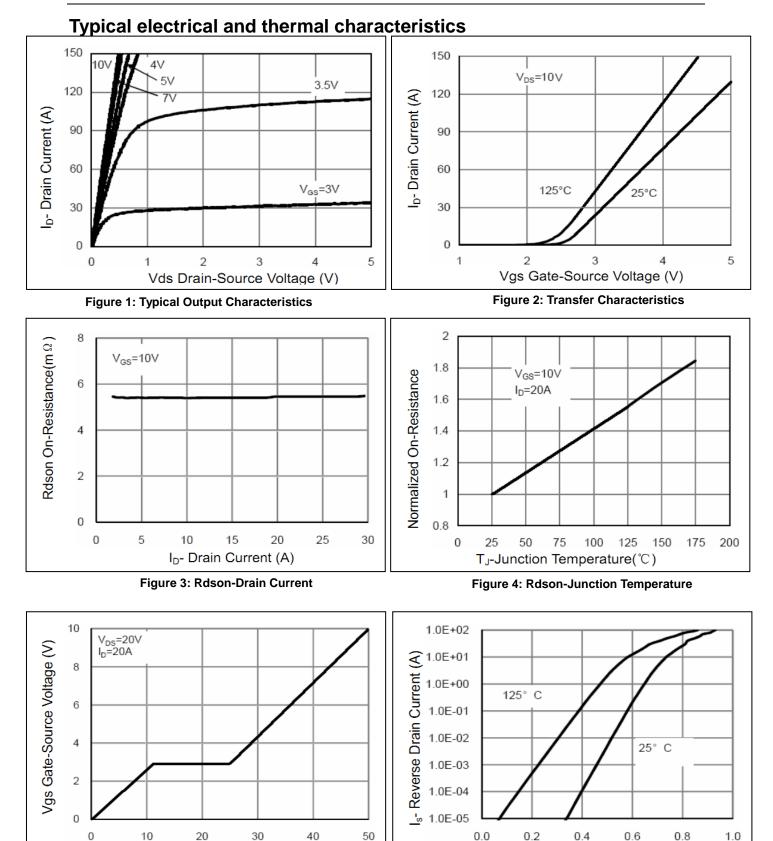


#### Notes:

- ①Calculated continuous current based on maximum allowable junction temperature.
- 2 Repetitive rating; pulse width limited by max. junction temperature.
- ③The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.



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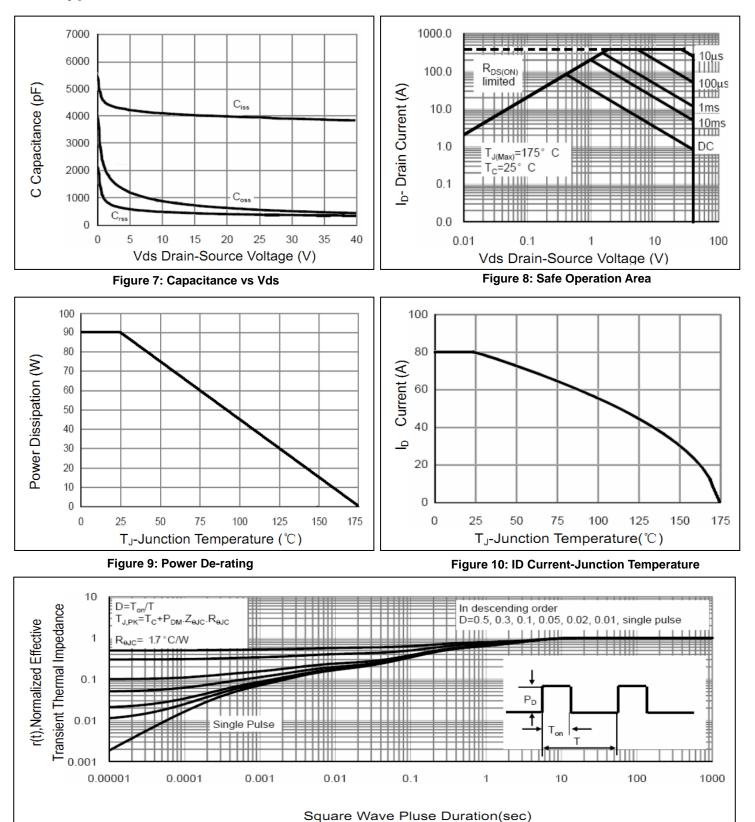




Vsd Source-Drain Voltage (V)



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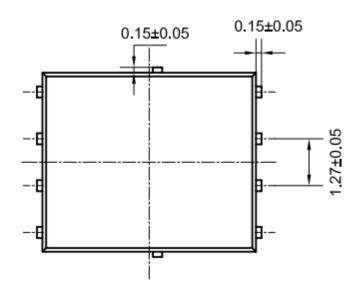


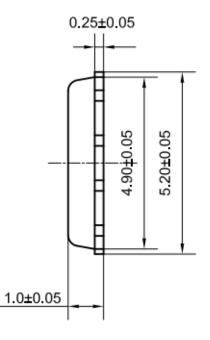
## Typical electrical and thermal characteristics

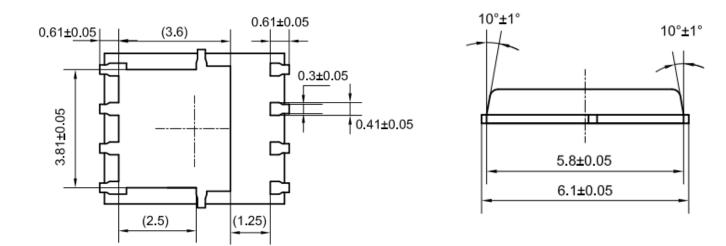




## **Mechanical Data:**









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